Claims

We claim:

1. A method of manufacturing an integrated circuit device, comprising:

forming an insulating layer on a substrate;

forming a capping layer on the insulating layer;

patterning the capping layer and the insulating layer; and

forming insulating spacers on sidewalls of the insulating layer such that the insulating layer is enclosed by the insulating spacers, the capping layer, and the substrate.

2. The method of Claim 1, wherein the insulating layer is a spin on glass layer.

3. The method of Claim 1, wherein the capping layer may comprise at least one of silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, or Al_2O_3.

4. The method of Claim 1, wherein the insulating layer is a first insulating layer, and wherein forming the insulating spacers comprises:

forming a second insulating layer on the capping layer, the sidewalls of the first insulating layer, and the substrate; and

etching the second insulating layer so as to expose the substrate and an upper surface of the capping layer, opposite the substrate.

5. The method of Claim 1, wherein each of the insulating spacers has a width in a range of about 50 Å to about 200 Å.

6. A method of manufacturing an integrated circuit device, comprising:

forming a pattern comprising a pair of mesa regions on a substrate;

forming a first insulating layer on the pair of mesa regions;

forming a second insulating layer on the pair of mesa regions and the substrate;

forming a capping layer on the second insulating layer;

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patterning the capping layer and the second insulating layer; and

forming insulating spacers on sidewalls of the second insulating layer such that the second insulating layer is enclosed by the insulating spacers, the capping layer, the first insulating layer, and the substrate.

7. The method of Claim 6, wherein the second insulating layer is a spin on glass layer.

8. The method of Claim 6, further comprising:

applying a cleaning solution to the integrated circuit device so as to expose a contact region between the pair of mesa regions by removing at least a portion of a native oxide layer from the contact region.

9. The method of Claim 8, wherein the cleaning solution comprises at least one of hydrofluoric (HF) acid or a mixture of NH_4OH, H_2O_2, and H_2O.

10. The method of Claim 6, further comprising:

forming a conductive layer on the pair of mesa regions and the substrate so as to fill a contact region between the pair of mesa regions and to cover the mesa regions; and

removing a portion of the conductive layer such that an upper surface of the first insulating layer, opposite the substrate, is exposed.

11. The method of Claim 10, wherein removing the portion of the conductive layer comprises:

chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed.

12. The method of Claim 6, wherein the capping layer may comprise at least one of silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, or Al_2O_3.

13. The method of Claim 6, wherein forming the insulating spacers comprises:

forming a third insulating layer on the capping layer, the sidewalls of the second insulating layer, and the substrate; and

etching the third insulating layer so as to remove at least a portion of the third insulating layer from the substrate and an upper surface of the capping layer, opposite the substrate.

14. The method of Claim 10, wherein each of the insulating spacers has a width in a range of about 50 Å to about 200 Å.

15. A method of manufacturing an integrated circuit device, comprising:

forming a pattern comprising a pair of mesa regions on a substrate;

forming a first insulating layer on the pair of mesa regions;

forming an etch stop layer on the substrate;

forming a second insulating layer on the pair of mesa regions and the etch stop layer;

forming a capping layer on the second insulating layer;

patterning the capping layer and the second insulating layer; and

forming insulating spacers on sidewalls of the second insulating layer such that the second insulating layer is enclosed by the insulating spacers, the capping layer, the first insulating layer, and the etch stop layer.

16. The method of Claim 15, wherein the second insulating layer is a spin on glass layer.

17. The method of Claim 15, wherein forming the insulating spacers comprises:

forming a third insulating layer on the capping layer, the sidewalls of the second insulating layer, and the etch stop layer; and

etching the third insulating layer so as to remove at least a portion of the third insulating layer from the second insulating layer and an upper surface of the capping layer, opposite the substrate.

18. The method of Claim 17, further comprising:

removing at least a portion of the etch stop layer from a contact region between the pair of mesa regions.

19. The method of Claim 18, further comprising:

applying a cleaning solution to the integrated circuit device so as to expose the contact region by removing at least a portion of a native oxide layer from the contact region.

20. The method of Claim 19, wherein the cleaning solution comprises at least one of hydrofluoric (HF) acid or a mixture of NH_4OH, H_2O_2, and H_2O.

21. The method of Claim 18, further comprising:

forming a conductive layer on the pair of mesa regions and the substrate so as to fill the contact region and to cover the mesa regions; and

removing a portion of the conductive layer such that an upper surface of the first insulating layer, opposite the substrate, is exposed.

22. The method of Claim 21, wherein removing the portion of the conductive layer comprises:

chemical mechanical polishing the conductive layer such that the upper surface of the first insulating layer, opposite the substrate, is exposed.

23. The method of Claim 15, wherein each of the insulating spacers has a width in a range of about 50 Å to about 200 Å.

24. The method of Claim 15, wherein the capping layer may comprise at least one of silicon oxide, silicon nitride, undoped polysilicon, doped polysilicon, or Al_2O_3.

25. A method of manufacturing an integrated circuit, comprising:

forming a gate electrode on a substrate;

forming a first insulating layer on the gate electrode;

forming a second insulating layer on the first insulating layer and the substrate;

forming a protective layer on the second insulating layer such that the second insulating layer is enclosed by the protective layer, the first insulating layer, and the substrate.

26. The method of Claim 25, wherein forming the protective layer comprises:

forming a capping layer on an upper surface of the second insulating layer, opposite the substrate; and

forming insulating spacers on sidewalls of the second insulating layer.

27. The method of Claim 25, further comprising:

forming a contact pad on the substrate that is self aligned by the gate electrode.

28. The method of Claim 25, wherein the second insulating layer is a spin on glass layer.